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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,634	02/09/2001	Erik R. Altman	YOR9-2000-0845 US1 (8728-	9328
7590 12/23/2003 F. CHAU & ASSOCIATES, LLP Suite 501 1900 Hempstead Turnpike East Meadow, NY 11554			EXAMINER WANG, ALBERT C	
			ART UNIT 2115	PAPER NUMBER 3
DATE MAILED: 12/23/2003				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/780,634

Applicant(s)

ALTMAN ET AL.

Examiner

Albert Wang

Art Unit

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 . 6) ☐ Other: .

DETAILED ACTION

1. Original claims 1-20 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Houston, U.S. Patent No. 6,307,281.

As per claim 9, Houston discloses a microprocessor, comprising:

a plurality of logic circuits divided into functional groups (Fig. 2, elements 36);

a selection device coupled to each of the functional groups, each selection device providing switching of on/off states of the corresponding functional group based on logical values stored in a register (Fig. 4, control interface 52 with register 56);

a program instruction which sets the logical values in the register to control the on/off states of the functional groups (Col. 5, lines 50-60, logic component 32 comprises software);
and

a compiler program which generates the logical values to be set in the register based on instruction sequences which anticipate usage of each of the functional groups (Col. 5, lines 60-67, logic component 32 used in combination with a compiler; Col. 6, line 60 – Col. 7, line 7).

As per claims 10, Houston discloses a switch which provides a connection from a supply voltage to a power line of the functional group in an on state (Fig. 4, switch 58).

As per claim 11, Houston discloses a switch which provides a connection from ground to a power line of the functional group in an on state (Fig. 4, switch 58).

As per claim 12, Houston discloses a register for each functional group (Fig. 2, a control interface 38 for each element 36).

As per claim 13, Houston discloses the register is updated after a number of instruction cycles (Col. 6, line 60 – Col. 7, line 7).

As per claim 14, Houston provides for an input table generated by the compiler program and including an instruction sequence and associated resource needs for the each of the functional groups wherein the usage of the functional groups is determined in accordance with the input table (Col. 5, lines 50-60).

As per claim 15, Houston discloses the usage of the functional groups includes usage of the functional groups after a number of instruction cycles (Col. 6, line 60 – Col. 7, line 7).

As per claim 16, Houston provides for an output table including logical states corresponding to power-saving on/off states of the functional groups (Col. 5, lines 50-60)

As per claims 1-8, since Houston discloses the microprocessor of claims 9-16, Houston discloses the claimed microprocessor.

3. Claims 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bartley, U.S. Patent No. 6,219,796.

As per claim 17, Bartley discloses a method for generating embedded instruction sequences to control power to logic circuits in a microprocessor, comprising the steps of:

generating an instruction sequence which controls a functional program for the microprocessor (Fig. 7, code sequence is generated prior to scan step; Col. 4, lines 15-19);

analyzing the instruction sequence to determine which of the logic circuits are active on each instruction cycle (Fig. 7, inactive segments are determined for each functional unit);

comparing a number of instruction cycles for which each logic circuit will be inactive after a current instruction cycle to a value for each instruction cycle of the functional program (Col. 7, lines 39-61, duration of inactive segments is compared to predetermined threshold); and

inserting instruction sequences to turn each of the logical circuits on or off based on the comparing step (Fig. 7, insert power-down/up instruction to functional unit).

As per claim 18, ~~Lin~~^{Bartley} discloses the method as recited in claim 17, wherein the step of inserting instruction sequences include programming a register with logical values wherein each of the logical circuits are turned on or off based on the logical values (Fig. 1, control registers 11f).

As per claim 19, Bartley discloses a number determined to provide net power savings in the logical circuits (Col. 7, lines 55-61).

As per claim 20, Bartley discloses a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine (Fig. 1, program memory 12)

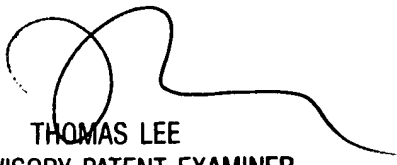
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

aw
December 15, 2003



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100